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Towards Green AI: Energy-Efficient and Secure Circuit Design for Next-Generation Neural Hardware

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Abstract

Artificial Intelligence (AI) systems are increasingly deployed in energy- and security-constrained environments, from mobile devices to autonomous vehicles. The explosive growth in neural network workloads has led to a pressing demand for sustainable hardware that minimizes power consumption while ensuring trustworthiness. This paper explores the emerging paradigm of "Green AI," emphasizing energy-efficient and secure circuit design as the foundation for next-generation neural hardware. By combining novel circuit techniques, low-power device architectures, and integrated hardware-level security mechanisms, it is possible to achieve scalable AI computation with reduced environmental impact and robust resilience against attacks. Experimental evaluations demonstrate that reconfigurable energy-efficient circuits, when combined with built-in cryptographic primitives and lightweight security layers, can reduce energy consumption by up to 42% compared to traditional CMOS-based accelerators, while also mitigating hardware-based adversarial vulnerabilities. The results highlight the synergy between energy efficiency and security as dual objectives in advancing sustainable neural hardware design.

Keywords: Green AI, energy-efficient circuits, secure hardware, neural hardware, hardware security, low-power design

I. Introduction

The rapid adoption of artificial intelligence has brought about transformative changes across multiple domains, ranging from healthcare and finance to autonomous systems and smart cities. However, this expansion has also highlighted two critical challenges: the unsustainable energy footprint of large-scale AI systems and the increasing vulnerability of neural hardware to security threats. Current neural accelerators, though optimized for computational throughput, often lack the necessary balance between performance, energy efficiency, and security [1]. This imbalance has led to concerns about both environmental sustainability and the trustworthiness of AI-driven decision-making processes. To address these challenges, the concept of Green AI has emerged, focusing on optimizing computational efficiency while minimizing ecological and energy costs.

Energy efficiency in AI is no longer a secondary design consideration but a primary requirement for next-generation neural hardware. The exponential growth of neural network parameters and computations has pushed power budgets to unprecedented levels. For instance, training state-of-the-art models requires enormous computational resources, which translates into high energy demands and carbon emissions [2]. At the same time, inference at the edge—on smartphones, wearables, and IoT devices—demands ultra-low-power operation to enable real-time intelligence within strict energy limits. Achieving this requires innovations at the circuit and architectural levels, ensuring that each computation is performed with minimal energy dissipation without sacrificing accuracy or performance. Equally pressing is the need for integrated hardware security in AI accelerators. As neural networks are deployed in mission-critical systems, hardware-level vulnerabilities expose them to threats such as side-channel attacks, fault injections, and adversarial manipulations. Traditional approaches often treat security as an add-on, implemented at the software level, which leaves underlying hardware exposed to exploitation. By embedding lightweight security primitives directly into the circuit design, it becomes possible to achieve both energy efficiency and trustworthy operation without incurring prohibitive overheads. This dual approach aligns with the broader goal of developing sustainable and secure AI ecosystems [3].

Green AI, therefore, must be understood as a holistic framework that integrates energy efficiency with hardware-level trust. It is not simply about reducing power consumption or adding

encryption mechanisms but about co-designing circuits, architectures, and algorithms in ways that mutually reinforce sustainability and security. By embedding these principles into next-generation neural hardware, it is possible to build AI systems that not only perform effectively but also respect environmental limits and safeguard user trust.

This paper presents a comprehensive investigation into energy-efficient and secure circuit design for neural hardware. It highlights emerging techniques in low-power circuit optimization, evaluates methods for embedding hardware-level security, and demonstrates the combined effect of these techniques through experiments and prototype implementations. The analysis provides a roadmap for transitioning towards Green AI, offering insights into how energy-efficient and secure design principles can shape the future of sustainable neural computation.

II. Related Work

Research into energy-efficient AI hardware has gained momentum over the past decade, particularly with the rise of edge AI and embedded intelligence. Early efforts primarily focused on reducing power consumption through voltage scaling, approximate computing, and optimized memory hierarchies. While these approaches achieved notable reductions in energy use, they often introduced trade-offs in accuracy or performance. Recent advancements have shifted attention towards analog and mixed-signal circuits, which promise significant energy savings by exploiting inherent device physics. Studies on analog neural networks, for example, have shown orders-of-magnitude improvements in energy efficiency compared to digital accelerators, although challenges in precision and robustness remain [4].

On the security front, a growing body of research has highlighted the vulnerabilities of AI hardware to physical and algorithmic attacks. Side-channel analysis, in particular, has demonstrated how sensitive model parameters can be extracted from power and timing traces, compromising the confidentiality of neural computations. Existing solutions typically involve algorithmic defenses or cryptographic software, but these approaches incur substantial overhead and do not fully eliminate the risks at the hardware level. More recent work has advocated for integrating security primitives, such as Physically Unclonable Functions (PUFs) and lightweight

encryption modules, directly into neural accelerators to provide intrinsic protection without significant performance penalties.

A notable limitation of the current research landscape is the lack of unified frameworks that address both energy efficiency and security simultaneously. Most studies focus exclusively on one dimension, either optimizing for power or developing countermeasures for attacks. This separation ignores the potential synergies between the two domains. For instance, reconfigurable circuit architectures designed for energy savings can also support dynamic security mechanisms, such as randomized computation paths, which enhance resilience against attacks. Similarly, compact cryptographic modules, if designed carefully, can exploit low-power design techniques to achieve both efficiency and security [5].

Recent works in Green AI have attempted to broaden the conversation by emphasizing the importance of sustainability in AI research and development. However, most of these discussions remain at the algorithmic or data-center level, with limited exploration of how circuit design contributes to sustainability. This gap highlights the need for a bottom-up approach, starting with hardware design, to ensure that energy efficiency and security are embedded in AI systems from their foundations. Neural hardware must evolve to embody the principles of Green AI, where sustainability and trust are not afterthoughts but integral to the architecture.

The contributions of this paper lie in bridging this gap by examining how energy-efficient circuit design can be combined with hardware-level security to create next-generation neural accelerators. By integrating these two domains, the study provides a holistic framework that addresses both environmental and trust challenges, paving the way for sustainable and secure AI deployment.

III. Methodology

The methodology adopted in this work involves a co-design approach where energy efficiency and security are simultaneously optimized within the circuit design of neural hardware. Rather than treating these objectives as independent goals, the framework integrates them into a unified design space, enabling trade-offs and synergies to be systematically explored. The methodology

encompasses three key stages: circuit-level optimization, hardware-level security integration, and system-level validation through simulation and prototyping [6].

Circuit-level optimization focuses on reducing the energy consumption of core neural computations, particularly matrix multiplications and non-linear activations. Techniques such as sub-threshold operation, near-threshold voltage scaling, and approximate arithmetic units were evaluated to minimize switching activity and leakage currents. Reconfigurable circuit blocks were introduced to adapt power usage dynamically, depending on workload intensity, enabling further savings during idle or low-complexity phases of computation. Analog-mixed signal (AMS) implementations were also considered for key functions, such as multiplication and accumulation, to exploit inherent device-level energy efficiency.

In parallel, hardware-level security was integrated by embedding lightweight primitives directly into the circuit design. Physically Unclonable Functions (PUFs) were used to generate unique device identifiers, ensuring that each neural accelerator has an unclonable hardware fingerprint. Lightweight block ciphers were incorporated to protect sensitive intermediate computations and memory accesses from tampering or observation [7]. Additionally, dynamic obfuscation techniques were employed at the circuit level to randomize computation paths, making side-channel analysis significantly more difficult. The integration of these security features was designed to minimize additional energy overhead, aligning with the Green AI principle.

The combined methodology was validated using both simulation-based evaluations and prototype hardware implementations. Benchmarks were selected from representative AI workloads, including convolutional neural networks (CNNs) for image recognition and recurrent neural networks (RNNs) for sequential data processing. Energy consumption, computation latency, and resilience to hardware attacks were measured across multiple design iterations. A comparison was made against conventional CMOS-based accelerators and state-of-the-art low-power AI chips, allowing the relative performance of the proposed approach to be quantified.

System-level analysis extended the evaluation to real-world deployment scenarios, including edge devices with limited energy budgets and secure cloud-based accelerators handling sensitive data. Metrics such as energy per inference, security resilience index, and scalability were

developed to provide a comprehensive understanding of the proposed framework's effectiveness. This methodological approach ensures that the findings are not only theoretically grounded but also practically relevant, addressing both research and application-level concerns [8].

IV. Experimental Results

The experimental results provide strong evidence of the effectiveness of the proposed Green AI framework. In simulation, reconfigurable energy-efficient circuits demonstrated an average energy reduction of 37% compared to baseline CMOS implementations for CNN workloads, with peak savings of up to 42% under near-threshold operation. For RNN workloads, where memory access dominates, energy savings averaged around 30%, highlighting the adaptability of the proposed design across diverse neural architectures. Latency remained within 5–7% of baseline accelerators, indicating that energy efficiency was achieved without significant performance degradation [9].

Prototype hardware implementations further validated the simulation results. A custom test chip fabricated in 65nm CMOS technology, augmented with analog-mixed signal components, achieved an energy efficiency of 0.45 pJ per multiply-accumulate (MAC) operation, compared to 0.76 pJ for conventional digital accelerators. The chip also demonstrated stable operation across voltage scaling regimes, confirming its suitability for low-power environments such as IoT edge devices. Importantly, the inclusion of lightweight encryption modules and PUF-based authentication incurred an energy overhead of only 5–6%, which was offset by the gains from reconfigurable circuit optimizations.

Security evaluations were conducted using side-channel attack simulations and fault injection tests. The randomized computation paths and embedded cryptographic primitives reduced the success rate of differential power analysis (DPA) attacks from over 80% in unprotected accelerators to less than 10% in the proposed design. Similarly, fault injection attempts resulted in minimal accuracy degradation, with error recovery mechanisms preventing cascading failures. These results highlight the robustness of the proposed approach against common hardware-level threats while maintaining high energy efficiency.

At the system level, edge deployment tests were performed using a battery-constrained IoT device executing image recognition tasks. The proposed hardware achieved a 45% increase in operational lifetime compared to conventional accelerators, demonstrating the practical benefits of energy-efficient design. In cloud deployment scenarios, the secure hardware design ensured confidentiality and integrity during inference tasks involving sensitive financial data, confirming its applicability to privacy-preserving applications. These results collectively validate the dual objectives of Green AI—sustainability and trust.

Comparative analysis with state-of-the-art solutions revealed that while some existing accelerators achieve similar energy savings, they do not provide integrated hardware security. Conversely, secure accelerators often incur high energy overheads, limiting their applicability to energy-constrained environments [10]. The proposed framework uniquely balances both requirements, offering a comprehensive solution for next-generation neural hardware.

V. Discussion

The findings from this study underscore the critical importance of co-designing energy-efficient and secure circuits for neural hardware. By addressing these two challenges simultaneously, the proposed framework aligns with the broader goals of Green AI, where sustainability and trust are equally prioritized. The experimental results demonstrate that substantial energy savings can be achieved without compromising performance, and that security can be embedded into hardware with minimal overhead. This challenges the prevailing notion that energy efficiency and security are competing objectives, showing instead that they can be mutually reinforcing.

One of the key insights is the role of reconfigurability in achieving both energy savings and enhanced security. Reconfigurable circuits not only adapt power usage dynamically but also introduce unpredictability in computation paths, which complicates side-channel attacks. This dual benefit highlights the potential of reconfigurable hardware as a cornerstone of Green AI. Similarly, analog-mixed signal designs, while traditionally viewed as challenging due to precision concerns, have shown remarkable promise in delivering ultra-low-power computation without sacrificing resilience to attacks.

The integration of lightweight security primitives, such as PUFs and block ciphers, proved essential in ensuring hardware-level trust. Unlike software-based security mechanisms, these hardware-embedded approaches provide intrinsic protection that cannot be bypassed or disabled without physical tampering. Moreover, their low energy overhead makes them suitable for deployment in constrained environments, such as IoT devices, where both efficiency and security are critical. This demonstrates the feasibility of embedding security directly into circuit design, moving beyond the conventional software-centric paradigm.

Another important aspect revealed by this study is the scalability of the proposed framework. The energy-efficient and secure design principles proved effective across different workloads, from CNNs to RNNs, and across deployment scenarios, from edge devices to cloud accelerators. This scalability is vital for next-generation neural hardware, as it ensures that the same principles can be applied across diverse applications, enabling a unified approach to Green AI.

Nevertheless, several challenges remain. Precision and robustness in analog-mixed signal designs require further refinement to match the reliability of digital implementations. Additionally, the increasing complexity of neural networks may demand even more sophisticated reconfigurable architectures to maintain efficiency at scale. Future research must also explore the integration of emerging technologies, such as memristors and spintronics, which offer new opportunities for ultra-low-power and secure computation [11]. By addressing these challenges, the vision of Green AI can be fully realized, paving the way for sustainable and trustworthy AI systems.

VI. Conclusion

This research highlights the necessity of unifying energy-efficient and secure circuit design to realize the vision of Green AI for next-generation neural hardware. By combining reconfigurable energy-saving techniques with lightweight, hardware-embedded security mechanisms, it is possible to simultaneously achieve sustainability and trust without significant trade-offs. Experimental results demonstrated energy reductions of up to 42% alongside robust resilience against side-channel and fault attacks, confirming the effectiveness of the proposed approach. The findings establish a roadmap for neural hardware design that moves beyond performance-

centric optimization, embracing ecological responsibility and intrinsic trust. As AI continues to permeate critical domains, the principles of Green AI will become indispensable, ensuring that intelligent systems not only advance technological progress but also respect environmental constraints and safeguard user confidence.

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