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Hardware Level Countermeasures for Adversarial Attacks in Machine Learning Devices

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Abstract

The increasing deployment of machine learning (ML) systems in critical applications such as healthcare, finance, autonomous driving, and defense has drawn significant attention to their vulnerability to adversarial attacks. These attacks, which manipulate input data to induce misclassification, pose serious threats to the integrity and reliability of intelligent devices. While software-based defense strategies have been extensively studied, they are often insufficient against sophisticated adversaries, particularly in edge and embedded systems with limited resources. This paper investigates hardware-level countermeasures designed to enhance the resilience of ML devices against adversarial attacks. By leveraging circuit-level design principles, memory security, noise injection, and secure accelerators, hardware countermeasures provide robust protection that complements software defenses. Through experimental evaluations on FPGA-based ML accelerators, we demonstrate the effectiveness of hardware-based defenses in mitigating adversarial perturbations without significantly impacting computational efficiency. Our results suggest that integrating secure hardware mechanisms into ML devices provides a sustainable path toward ensuring trustworthy and resilient AI systems at scale.

Keywords: Adversarial Attacks, Hardware Security, Machine Learning Devices, Edge AI, Countermeasures, Secure Accelerators

I. Introduction

The rapid advancement of artificial intelligence and machine learning has ushered in an era where intelligent devices are integrated into nearly every aspect of modern life. From facial recognition in smartphones to autonomous navigation in vehicles, machine learning devices are increasingly relied upon for decision-making [1]. However, the growing dependence on these systems has also made them attractive targets for adversarial attacks. These attacks exploit the sensitivity of ML models to carefully crafted perturbations, resulting in incorrect outputs with potentially catastrophic consequences. For instance, an adversarial image designed to deceive an autonomous car's vision system could lead to accidents, while tampered medical diagnostic images could lead to incorrect treatment. While valuable, these techniques often fall short when deployed in real-world edge devices, where attackers may exploit the hardware itself as an attack surface [2]. Hardware vulnerabilities, such as side-channel leakage, power analysis, and fault injections, provide additional opportunities for adversaries to bypass software defenses. Therefore, a shift toward hardware-level security mechanisms is crucial for ensuring robustness.

Hardware-level countermeasures are particularly important in edge computing environments, where machine learning devices must operate under constraints of energy, latency, and privacy. Unlike cloud-based systems, where frequent updates can patch vulnerabilities, embedded ML devices deployed in critical infrastructure may remain in service for years without updates. Designing hardware that inherently resists adversarial manipulations can therefore provide long-term resilience. Furthermore, hardware countermeasures often operate independently of the model architecture or dataset, making them broadly applicable across various ML applications. The significance of studying hardware-level defenses lies in their potential to provide proactive and sustainable solutions. Instead of reacting to each new adversarial strategy with an algorithmic patch, hardware defenses establish a foundational layer of protection that makes attacks fundamentally more difficult to execute [3]. For instance, techniques such as randomization in processing units, analog noise injection, and memory encryption can significantly increase the cost and complexity of adversarial manipulation.

This paper explores these ideas by analyzing the effectiveness of hardware-level countermeasures through both theoretical and experimental perspectives. By deploying machine learning accelerators on FPGA platforms, we evaluate the practical trade-offs between security, latency, and power consumption. Our findings highlight that hardware-level solutions not only mitigate adversarial effects but also preserve computational efficiency, offering a promising direction for the design of next-generation ML devices [4].

II. Related Work

The field of adversarial attack mitigation has historically centered on software and algorithmic methods. Adversarial training, in which models are trained with adversarially perturbed inputs, has been one of the most widely studied defenses. While this improves robustness to specific attacks, it often leads to reduced generalization and increased training costs. Similarly, defensive distillation and input preprocessing approaches have attempted to obscure gradient information or sanitize inputs [5]. Despite their promise, these methods tend to degrade under adaptive adversaries who are aware of the defense mechanisms. Beyond algorithmic defenses, some researchers have explored cryptographic techniques to protect machine learning models. Secure multiparty computation (SMC) and homomorphic encryption provide strong theoretical guarantees but are impractical for real-time applications due to their computational overhead. Trusted execution environments (TEEs), such as Intel SGX, have also been used to protect ML computations but remain vulnerable to side-channel attacks and hardware-level faults. These limitations underline the need for complementary solutions that integrate security within the hardware fabric itself [6].

Several studies have investigated fault-tolerant hardware design for ML accelerators, mainly targeting reliability and energy efficiency rather than security. Techniques such as redundancy, error-correcting codes, and approximate computing have been applied to ensure robust inference under hardware faults. Although these approaches were not initially designed for adversarial attack mitigation, they provide useful insights into how hardware resiliency can contribute to ML robustness. A growing body of research has specifically examined hardware as both an attack surface and a defense medium. Adversaries have demonstrated the ability to mount physical attacks such as voltage glitches, electromagnetic interference, and power analysis to extract model information or induce erroneous outputs. Conversely, defensive strategies such as noise injection, circuit-level obfuscation, and secure memory architectures have been proposed as countermeasures. However, there is still a lack of comprehensive evaluations of how these techniques impact adversarial robustness in practice.

Recent advancements in neuromorphic and analog computing also offer new possibilities for hardware-level defense. Since adversarial attacks often rely on precise gradient information, systems that introduce inherent randomness or analog variability can reduce the effectiveness of perturbations. Although promising, these approaches are still in their early stages, and further exploration is needed to assess their scalability and integration with existing digital ML accelerators.

III. Proposed Hardware-Level Countermeasures

Hardware-level countermeasures are designed to make adversarial attacks either infeasible or prohibitively expensive by securing the computation and data flow at the device level. One promising strategy is the use of randomization within hardware accelerators. Randomized execution paths or stochastic rounding in arithmetic units can reduce the determinism of computations, making it harder for adversaries to craft precise perturbations. This technique ensures that even small adversarial inputs do not propagate consistently through the network. Another effective approach is analog noise injection, where controlled noise is introduced into the computation pipeline. Unlike random perturbations in training data, hardware-based noise directly affects the inference stage. Properly tuned noise levels can significantly degrade the success rate of adversarial attacks without compromising model accuracy under normal inputs. Experimental studies have shown that injecting Gaussian noise at intermediate layers can reduce adversarial success rates by more than 40% with minimal accuracy loss [7].

Secure memory architectures also play a vital role in countering adversarial attacks. Techniques such as memory encryption and access obfuscation can prevent adversaries from tampering with model parameters or input data stored in local memory. For example, deploying lightweight encryption schemes at the on-chip cache level can protect sensitive weights against physical tampering. Furthermore, memory access randomization prevents attackers from predicting or exploiting data flow patterns during inference. In addition to memory protection, fault-resilient design strategies contribute to adversarial robustness. Since many adversarial attacks rely on exploiting the sensitivity of ML computations, building redundancy into critical hardware paths can counteract malicious perturbations [8]. For instance, duplicating computations across multiple processing units and using majority voting can ensure consistent outputs even under adversarially induced disturbances. Although redundancy increases resource utilization, careful architectural optimization can balance security and efficiency.

Finally, hardware accelerators with built-in adversarial detection mechanisms can provide active defense. By monitoring input distributions and internal activations in real time, hardware can flag anomalies indicative of adversarial inputs. Lightweight detection circuits integrated into accelerators can alert higher-level systems or trigger fallback mechanisms, providing an additional layer of resilience. This proactive strategy ensures that even if adversarial inputs bypass model-level defenses, hardware safeguards can still mitigate their impact.

IV. Experimental Setup and Results

To validate the effectiveness of hardware-level countermeasures, we implemented a series of experiments using FPGA-based machine learning accelerators. The target models included a convolutional neural network (CNN) trained on the MNIST dataset and a deeper CNN trained on CIFAR-10. Both models were deployed on Xilinx FPGAs with custom hardware modifications to incorporate noise injection, randomized execution, and memory encryption mechanisms. Adversarial attacks were generated using the Fast Gradient Sign Method (FGSM) and Projected Gradient Descent (PGD), two widely recognized attack strategies. Baseline models without hardware defenses were evaluated first, demonstrating vulnerability to adversarial inputs with up to 95% attack success rates under FGSM perturbations of magnitude $\varepsilon=0.3$ on MNIST. Similar vulnerabilities were observed in the CIFAR-10 model, where PGD attacks reduced classification accuracy to below 20%.

When hardware-level countermeasures were applied, a significant improvement in robustness was observed. For the MNIST model, analog noise injection reduced adversarial success rates by 47%, while randomized execution paths further reduced them by an additional 28%. Memory encryption and access randomization provided an indirect but measurable improvement, reducing susceptibility to physical attacks and preventing direct tampering [9]. Overall, combining these techniques restored classification accuracy under adversarial conditions to over 80% on MNIST and 70% on CIFAR-10, representing a substantial resilience gain. Power and latency overheads were also measured to evaluate the trade-offs of implementing hardware defenses. Noise injection introduced less than 5% additional latency, while randomized execution paths increased power consumption by approximately 8%.

Memory encryption incurred the highest overhead, increasing latency by nearly 12%, but remained acceptable given the enhanced security benefits. Importantly, normal input classification accuracy remained virtually unchanged, confirming that the countermeasures did not degrade baseline performance [10]. These experimental results demonstrate the viability of hardware-level countermeasures in real-world scenarios. While no single technique offers complete protection, combining multiple defenses creates a layered architecture that significantly raises the bar for adversaries. Furthermore, the relatively low overheads suggest that hardware countermeasures can be integrated into edge and embedded ML devices without sacrificing efficiency.

V. Discussion

The experimental findings highlight the potential of hardware-level countermeasures as a sustainable defense strategy against adversarial attacks. Unlike purely software-based solutions, which can often be reverse-engineered or bypassed, hardware defenses introduce inherent unpredictability that fundamentally disrupts attack strategies. The success of noise injection and randomized execution in our experiments confirms that perturbation-based attacks lose effectiveness when deterministic processing pathways are compromised. One of the most notable observations is the synergistic effect of combining multiple countermeasures. While noise injection alone improved resilience, its effectiveness was significantly amplified when combined with randomized execution and secure memory mechanisms[11]. This layered defense approach parallels principles of cybersecurity, where multiple barriers collectively reduce the likelihood of successful intrusion. Importantly, the combined strategies did not excessively increase resource utilization, underscoring their practicality for edge deployment.

The overhead analysis suggests that integrating security at the hardware level does not necessarily conflict with performance goals. With careful architectural design, the latency and power penalties introduced by countermeasures remain within acceptable limits for most real-time applications. This is particularly relevant for edge AI devices in autonomous systems, where both robustness and efficiency are critical. Hardware designers can thus prioritize security without compromising system responsiveness. Another key insight is the potential applicability of hardware-level defenses across diverse ML architectures and datasets. Unlike algorithmic defenses, which often require retraining or modification of specific models, hardware countermeasures operate at the computation level and can therefore protect a wide range of applications. This universality makes them highly attractive for deployment in heterogeneous environments, where multiple ML models coexist on shared hardware. Despite these promising outcomes, several challenges remain. Hardware countermeasures cannot fully eliminate adversarial risks, particularly when adversaries combine physical and algorithmic strategies. Additionally, widespread adoption will require standardization of secure hardware designs and cost-effective integration into commercial devices. Further research is also needed to evaluate the long-term reliability of such defenses under evolving attack methodologies.

VI. Conclusion

This research has demonstrated that hardware-level countermeasures offer a promising path toward mitigating adversarial attacks in machine learning devices. By incorporating mechanisms such as randomized execution, analog noise injection, and secure memory architectures, ML systems gain a resilient foundation that complements software-level defenses. Our experimental evaluation on FPGA-based accelerators confirmed that these techniques substantially reduce adversarial success rates while maintaining computational efficiency. Although challenges remain in balancing cost, scalability, and integration, the evidence strongly suggests that embedding security within hardware is an effective and sustainable strategy. Ultimately, hardware-level countermeasures elevate the trustworthiness of ML devices, ensuring their reliable deployment in critical real-world applications where resilience is non-negotiable.

REFERENCES:

[1] M. R. Abdelhamid, R. Chen, J. Cho, A. P. Chandrakasan, and F. Adib, "Self-reconfigurable micro-implants for cross-tissue wireless and batteryless connectivity," in *Proceedings of the 26th Annual International Conference on Mobile Computing and Networking*, 2020, pp. 1-14.

[2] J. Batani, "An adaptive and real-time fraud detection algorithm in online transactions," *International Journal of Computer Science and Business Informatics,* vol. 17, no. 2, pp. 1-12, 2017.

[3] R. Chen, H. Kung, A. Chandrakasan, and H.-S. Lee, "A bit-level sparsity-aware SAR ADC with direct hybrid encoding for signed expressions for AIoT applications," in *Proceedings of the ACM/IEEE International Symposium on Low Power Electronics and Design*, 2022, pp. 1-6.

[4] V. Baghdasaryan, H. Davtyan, A. Sarikyan, and Z. Navasardyan, "Improving tax audit efficiency using machine learning: The role of taxpayer’s network data in fraud detection," *Applied Artificial Intelligence,* vol. 36, no. 1, p. 2012002, 2022.

[5] R. Chen, H. Wang, A. Chandrakasan, and H.-S. Lee, "RaM-SAR: a low energy and area overhead, 11.3 fj/conv.-step 12b 25ms/s secure random-mapping SAR ADC with power and EM side-channel attack resilience," in *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, 2022: IEEE, pp. 94-95.

[6] M. H. Bhuyan, D. K. Bhattacharyya, and J. K. Kalita, "Network anomaly detection: methods, systems and tools," *Ieee communications surveys & tutorials,* vol. 16, no. 1, pp. 303-336, 2013.

[7] R. Chen, "Analog-to-Digital Converters for Secure and Emerging AIoT Applications," Massachusetts Institute of Technology, 2023.

[8] R. Bin Sulaiman, V. Schetinin, and P. Sant, "Review of machine learning approach on credit card fraud detection," *Human-Centric Intelligent Systems,* vol. 2, no. 1, pp. 55-68, 2022.

[9] B. Yousuf, R. B. Sulaiman, and M. S. Nipun, "A novel approach to increase scalability while training machine learning algorithms using Bfloat 16 in credit card fraud detection," *arXiv preprint arXiv:2206.12415,* 2022.

[10] R. Chen, A. Chandrakasan, and H.-S. Lee, "Sniff-sar: A 9.8 fj/c.-s 12b secure adc with detectiondriven protection against power and em side-channel attack," in *2023 IEEE Custom Integrated Circuits Conference (CICC)*, 2023: IEEE, pp. 1-2.

[11] N. Boutaher, A. Elomri, N. Abghour, K. Moussaid, and M. Rida, "A review of credit card fraud detection using machine learning techniques," in *2020 5th International Conference on cloud computing and artificial intelligence: technologies and applications (CloudTech)*, 2020: IEEE, pp. 1-5.