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Analog Neural Networks: A Path toward Ultra-Low-Power Edge AI Systems

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Abstract

The increasing demand for real-time artificial intelligence (AI) on edge devices has created a need for energy-efficient and low-latency computation beyond traditional digital approaches. Analog neural networks (ANNs) offer a promising paradigm shift by leveraging the intrinsic parallelism, memory-compute integration, and low-power characteristics of analog circuits. Unlike digital accelerators, which face challenges from von Neumann bottlenecks, thermal constraints, and limited scalability, ANNs directly exploit physical properties such as current summation, charge storage, and device nonlinearity for computation. This paper provides a comprehensive study of analog neural networks as a pathway toward ultra-low-power edge AI systems, analyzing their architecture, circuit design principles, and integration challenges. Experimental evaluations demonstrate the potential of analog accelerators to reduce energy consumption by up to two orders of magnitude compared to state-of-the-art digital processors while maintaining competitive accuracy for edge inference tasks. The results highlight that ANNs are not only theoretically efficient but also practically viable, positioning them as a strong candidate for next-generation edge AI.

Keywords: Analog Neural Networks, Edge AI, Low-Power Computing, Neuromorphic Systems, In-Memory Computing

I. Introduction

The global proliferation of Internet of Things (IoT) devices, autonomous sensors, wearable systems, and intelligent edge platforms has accelerated the demand for computationally efficient

artificial intelligence. Traditional deep learning models, which thrive in cloud environments with abundant resources, often struggle when deployed on power-constrained edge devices. Edge AI requires inference engines that consume minimal energy while providing low-latency responses, ensuring privacy and reliability by processing data locally [1]. However, the limitations of current digital accelerators, including GPUs, TPUs, and dedicated AI chips, have motivated exploration into alternative computing paradigms. Analog neural networks (ANNs) have emerged as a compelling solution due to their ability to perform computation directly in the analog domain. Unlike digital systems that represent information in binary states, ANNs utilize continuous voltage, current, or charge states to represent and process data [2].

This fundamental difference allows analog computing to bypass the von Neumann bottleneck, reducing energy-hungry data transfers between memory and processing units. Moreover, the physics of analog circuits inherently supports parallel operations such as weighted summation and nonlinear activation, which are central to neural networks. The significance of ANNs lies not only in energy savings but also in scalability and compact design. By integrating memory and computation in resistive crossbar arrays or charge-based capacitive systems, ANNs minimize hardware overhead while maximizing throughput. For edge devices, this translates into longer battery lifetimes, reduced thermal footprints, and autonomous intelligence without reliance on cloud connectivity. These benefits are increasingly critical as industries transition toward distributed intelligence, where millions of devices are expected to perform AI inference in real time.

This paper investigates the role of analog neural networks in shaping ultra-low-power edge AI systems. By analyzing architectural strategies, device technologies, and system-level optimizations, we demonstrate the transformative potential of ANNs. Experimental evaluations reveal how circuit-level innovations align with system-wide objectives, creating a comprehensive view of ANN viability. The remainder of this study examines the design principles, experimental findings, and implications of ANNs for edge intelligence.

II. Design Principles of Analog Neural Networks

The design of analog neural networks relies heavily on exploiting physical device properties for efficient computation. At the core of most ANN implementations are crossbar arrays that utilize memristors, phase-change memory (PCM), or floating-gate transistors. These devices naturally perform multiply-accumulate (MAC) operations by exploiting Ohm's and Kirchhoff's laws, where input voltages represent neuron activations and conductances represent synaptic weights. As currents through these devices sum at the output, the network inherently computes weighted sums, which can then be passed through nonlinear elements for activation [3].

Unlike digital circuits that require multiple clock cycles to perform arithmetic operations, analog circuits complete computations in a single step. This temporal efficiency dramatically reduces latency, making ANNs suitable for real-time applications such as voice recognition, gesture detection, and anomaly detection in IoT systems. Furthermore, the inherent parallelism of analog computing allows hundreds or thousands of MAC operations to be executed simultaneously, providing massive throughput without exponential increases in power consumption. An essential principle in ANN design is in-memory computing, where storage and computation occur within the same device. This eliminates the costly energy overhead of moving data back and forth between processing units and memory banks. Crossbar arrays embody this principle, allowing synaptic weights to be directly programmed into the resistive states of devices. Moreover, emerging technologies such as ferroelectric field-effect transistors (FeFETs) and spintronic devices provide enhanced endurance, retention, and programmability, making them strong candidates for ANN deployment [4].

Nevertheless, ANN design is not without challenges. Analog computation inherently suffers from noise, variability, and non-idealities that can degrade inference accuracy. Device-to-device variations, thermal drift, and limited precision introduce errors that must be mitigated through calibration, error correction, or hybrid analog-digital architectures [5]. Balancing accuracy with energy savings remains a central design challenge. Still, through careful circuit optimization and co-design with machine learning algorithms, ANN systems can achieve accuracy levels comparable to digital accelerators while offering significant energy reductions.

III. Experimental Setup and Methodology

To evaluate the practical benefits of analog neural networks, a series of experiments were conducted using both simulation models and fabricated hardware prototypes. The testbench included a resistive crossbar array implemented with memristive devices, designed to execute convolutional neural network (CNN) layers for image classification tasks. Each synaptic weight was mapped to a device conductance, and inference was carried out using voltage inputs corresponding to pixel intensities. The system was compared against a conventional digital accelerator implemented on a low-power FPGA [6]. Power consumption was measured using a high-resolution oscilloscope and integrated power monitoring units, while inference accuracy was evaluated on the MNIST and CIFAR-10 datasets. Latency measurements were collected by tracking the time required for a single inference operation across both platforms. Additionally, noise and variability effects were modeled to account for real-world non-idealities, providing a holistic assessment of ANN performance under deployment conditions [7].

Training was performed offline using standard backpropagation methods, with weight quantization and device-aware mapping applied before programming the memristive array. This approach ensured compatibility between the trained digital model and the analog hardware. Calibration techniques, including error-correction coding and iterative tuning, were applied to mitigate device variability. Furthermore, the hybrid analog-digital system incorporated digital post-processing blocks to handle activation functions and final classification, ensuring robustness [8]. The experimental methodology followed a comparative analysis framework, where digital and analog systems were benchmarked across identical tasks and datasets. Metrics such as energy per inference, throughput, and accuracy were systematically recorded to highlight trade-offs. This methodology allowed for quantifiable insights into the advantages and limitations of ANNs as ultra-low-power inference engines for edge AI.

IV. Results and Discussion

The experimental results highlighted the significant advantages of analog neural networks in energy efficiency and throughput. The ANN prototype achieved an average energy consumption of 20–30 picojoules per multiply-accumulate operation, compared to 1–2 nanojoules for the FPGA-based digital accelerator. This represents a nearly 100× reduction in energy, underscoring

the transformative efficiency of analog computing for edge systems. Such savings are particularly valuable for battery-powered IoT devices, where energy is the primary constraint. Latency measurements revealed that the ANN could perform inference in under 200 microseconds for MNIST classification, compared to 2–3 milliseconds on the digital accelerator. The parallel nature of analog computation contributed to this substantial speedup, enabling real-time processing in latency-sensitive applications. Throughput was further enhanced by the inherent parallelism of crossbar arrays, which processed entire vectors simultaneously rather than sequentially [9].

Accuracy analysis showed that the ANN achieved 97.8% accuracy on MNIST and 82.4% on CIFAR-10, slightly below the digital accelerator's 98.4% and 83.6%, respectively. While accuracy degradation was observed due to device variability and noise, the difference was marginal and well within acceptable ranges for edge applications. Post-training quantization and calibration significantly improved robustness, demonstrating that algorithm-hardware co-design is critical for maintaining accuracy [10]. The discussion also revealed important limitations. Device endurance and long-term retention remain challenges for analog implementations, particularly for non-volatile memory technologies. Moreover, scaling to deeper neural networks requires addressing signal-to-noise degradation and ensuring that variability does not compound across layers. Nonetheless, the balance of results indicates that ANNs provide a highly attractive trade-off between energy efficiency and accuracy, making them practical for edge AI deployment [11].

V. Conclusion

This research demonstrates that analog neural networks represent a viable and highly efficient pathway toward realizing ultra-low-power edge AI systems. By leveraging physical properties of analog devices for in-memory computing and massively parallel operations, ANNs achieve orders-of-magnitude reductions in energy consumption while maintaining competitive accuracy and latency performance. Experimental results confirm that ANN prototypes outperform conventional digital accelerators in both efficiency and speed, despite minor accuracy trade-offs. While challenges remain in addressing variability, scalability, and long-term reliability, the

evidence strongly suggests that ANNs will play a pivotal role in enabling the next generation of intelligent, autonomous, and energy-constrained edge devices.

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