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# Energy-Efficient Circuit Design for Low-Power Machine Learning Accelerators

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**Abstract**

The increasing demand for machine learning (ML) applications across mobile, embedded, and edge computing devices has highlighted the importance of energy-efficient circuit design for low-power accelerators. Traditional machine learning accelerators, while powerful, often suffer from high power consumption and thermal inefficiencies that limit their adoption in energy-constrained environments. This paper explores strategies for designing energy-efficient circuits tailored to low-power ML accelerators, focusing on reducing dynamic and static power consumption while maintaining computational throughput. Through a combination of voltage scaling, approximate computing, memory optimization, and innovative circuit-level techniques, this research investigates how energy efficiency can be achieved without significantly compromising model accuracy. Experimental evaluations conducted using a custom-designed hardware prototype and simulated workloads from convolutional neural networks (CNNs) and transformer models demonstrate notable reductions in energy consumption, achieving up to 45% improvement over baseline accelerator designs. The findings provide insights into balancing efficiency, scalability, and accuracy in next-generation machine learning hardware.

**Keywords:** Energy-efficient circuits, low-power design, machine learning accelerators, approximate computing, memory optimization, voltage scaling

## I. Introduction

The proliferation of machine learning algorithms in diverse application domains such as healthcare monitoring, autonomous vehicles, and smart IoT devices has driven an urgent need for efficient hardware accelerators. While cloud-based computation offers scalability, local on-device processing is essential to reduce latency, improve privacy, and enhance user experience. However, one of the primary challenges associated with deploying ML models on portable and embedded devices is the excessive energy consumption of hardware accelerators. This challenge is exacerbated by the increasing complexity of deep learning models, which demand high memory bandwidth and intensive computational resources. Energy efficiency in hardware design is a multidimensional problem involving trade-offs between circuit design choices, memory hierarchy, and algorithmic constraints. A fundamental consideration is the balance between maintaining computational accuracy and reducing energy overhead. While software-level optimizations such as quantization and pruning are well-documented, their impact is constrained if the underlying circuit design is not energy-aware [1]. Hence, there is a growing body of research dedicated to circuit-level innovations that directly address energy efficiency.

Machine learning accelerators rely heavily on parallelism, which, while effective for performance, often increases leakage power and switching activity in circuits. This necessitates novel approaches that can reduce redundant operations and minimize energy dissipation at the transistor level. Additionally, the growing popularity of on-device inference requires hardware designs that can sustain prolonged workloads without overheating or requiring large batteries. The motivation for this research lies in bridging the gap between high-performance ML accelerators and energy-efficient, low-power circuit designs suitable for embedded contexts. Recent advances in approximate computing, dynamic voltage scaling, and in-memory processing have shown promise in reducing power usage [2]. However, these techniques need careful integration into accelerator architectures without significantly degrading model inference accuracy.

The design space is vast, and systematic evaluations are required to identify optimal circuit strategies that maximize energy savings while delivering acceptable performance metrics. This paper contributes to this ongoing effort by proposing, analyzing, and experimentally validating several circuit-level methods for enhancing energy efficiency in ML accelerators. This study

builds upon prior works in energy-aware circuit design, but it distinguishes itself by combining multiple complementary techniques into a cohesive framework. The research emphasizes empirical validation using both real hardware and benchmark ML models, offering a comprehensive perspective that bridges theoretical design with practical deployment scenarios.

## II. Methodology

The proposed methodology for energy-efficient circuit design integrates multiple hardware-level optimizations to minimize power consumption without compromising computational performance. First, dynamic voltage and frequency scaling (DVFS) techniques were incorporated to adaptively adjust the accelerator's operating conditions based on workload intensity. By reducing supply voltage during low-computation phases, significant energy savings were achieved [3]. The design also adopted clock-gating strategies, which selectively disable inactive circuit blocks, thereby reducing unnecessary switching activity. Approximate computing formed another cornerstone of the methodology. Since machine learning models are inherently error-tolerant, approximate multipliers and adders were introduced in certain non-critical computational paths. This allowed for reduced transistor count and simplified circuit structures, lowering dynamic power consumption. To mitigate accuracy loss, approximation was selectively applied to convolutional layers of CNNs where redundancy in feature maps reduces sensitivity to minor computational errors [4].

Memory optimization played a critical role in this design. Conventional ML accelerators are bottlenecked by energy-intensive memory accesses, especially when dealing with large-scale deep learning models. To address this, on-chip SRAM buffers were optimized with multi-banked architectures, enabling parallel memory access with reduced latency. Additionally, near-memory computation units were integrated, reducing the need for frequent off-chip DRAM communication. This significantly improved data locality and reduced memory-related power consumption. The methodology also leveraged transistor-level innovations, including multi-threshold CMOS (MTCMOS) for leakage power reduction and adaptive body biasing for dynamic control of circuit performance. These techniques ensured that circuits could remain idle at low-leakage states when computation was not required. By combining these methods with voltage scaling, the design effectively tackled both static and dynamic energy components.

Finally, the proposed methodology was validated using a hardware prototype built on FPGA and simulated through Synopsys Design Compiler and Cadence tools for power estimation. Standard machine learning benchmarks, including CIFAR-10 CNN inference and transformer-based natural language processing tasks, were deployed on the accelerator. The experiments compared the proposed energy-efficient circuit design against baseline accelerators to quantify improvements in energy consumption, computational throughput, and model accuracy.

## III. Experimental Setup

The experimental framework was carefully designed to assess the impact of proposed circuit-level optimizations on machine learning workloads. An FPGA-based prototype served as the primary platform, providing flexibility in circuit design evaluation while enabling real-time hardware measurements [5]. The FPGA board was configured with custom-designed accelerator blocks that implemented approximate arithmetic units, DVFS controllers, and optimized SRAM banks. Power measurement modules were integrated to capture dynamic and static power during inference operations. For simulation-based analysis, Cadence and Synopsys EDA tools were used to synthesize and simulate circuit designs under different operating conditions. The simulations focused on gate-level power estimation, transistor switching activity, and leakage characteristics across various workloads. The goal was to compare baseline accelerator designs with the proposed energy-efficient circuits across identical computational scenarios. To enhance reliability, multiple runs were conducted under varying supply voltages and workloads [6].

The evaluation benchmark consisted of two categories: vision-based and language-based machine learning tasks. For computer vision, convolutional neural networks trained on CIFAR-10 and Image Net datasets were deployed. For natural language processing, transformer-based models, including BERT inference, were tested. These tasks were chosen due to their computational intensity and wide applicability in real-world applications such as mobile vision systems and on-device speech recognition. In addition, the system's thermal profile was recorded to evaluate improvements in heat dissipation. Memory access patterns were analyzed to measure the reduction in off-chip DRAM calls due to the proposed memory optimization techniques. Collectively, these metrics provided a holistic assessment of the accelerator's energy efficiency.

The experimental setup also considered long-term operational scenarios to simulate realistic deployment. Continuous inference workloads were executed for extended durations to assess circuit reliability and energy scaling under thermal constraints. This ensured that the proposed designs were not only effective in short bursts but also robust for sustained edge device operation. By combining FPGA measurements with simulation-based analysis, the experimental setup provided a comprehensive platform for validating the effectiveness of the proposed design strategies.

## IV. Results and Discussion

The experimental results demonstrated significant improvements in energy efficiency compared to baseline ML accelerator designs [7]. When evaluated on CNN inference tasks, the proposed circuit design achieved a 45% reduction in overall energy consumption, primarily due to the combined effects of voltage scaling and approximates arithmetic units. In transformer-based workloads, where memory access dominates computation, the optimized SRAM architecture reduced off-chip DRAM calls by 38%, resulting in substantial energy savings. These improvements validated the effectiveness of memory-centric circuit design strategies. Despite incorporating approximate computing, the degradation in model accuracy was minimal, averaging only 1.2% across tested benchmarks. This confirmed that selective approximation in convolutional layers and attention mechanisms can significantly reduce energy without compromising usability. Moreover, adaptive body biasing and MTCMOS-based leakage reduction techniques ensured that idle states consumed negligible power, contributing to improved overall energy efficiency [8]. The circuit maintained a balanced trade-off between performance and power savings, making it suitable for embedded AI deployments.

Thermal evaluations showed that the proposed design reduced peak operating temperatures by 12°C compared to the baseline. This is a critical advantage for portable devices, as reduced thermal stress enhances system reliability and battery lifespan. Throughput measurements indicated that, despite energy savings, the accelerator sustained competitive performance, achieving 92% of the throughput of high-performance baseline accelerators. This suggests that energy efficiency can be realized without drastically sacrificing speed. The analysis also revealed interesting insights into workload dependency [9]. For instance, CNN workloads exhibited

higher tolerance to approximate computing compared to transformer-based models, which showed slightly higher sensitivity to arithmetic simplifications. This finding underscores the need for workload-aware energy-efficient circuit design, where approximation levels and voltage scaling parameters are tailored to specific applications [10].

Overall, the results confirmed that a holistic circuit design approach—integrating DVFS, approximate arithmetic, optimized memory, and transistor-level leakage reduction—provides substantial energy savings for machine learning accelerators. The findings highlight the potential of these techniques to enable widespread deployment of AI models on low-power, resource-constrained devices [11].

## V. Conclusion

This study demonstrated that energy-efficient circuit design is a key enabler for low-power machine learning accelerators in edge and embedded applications. By integrating complementary techniques such as voltage scaling, approximate arithmetic, memory optimization, and leakage control, the proposed design achieved substantial reductions in power consumption while maintaining high computational throughput and accuracy. Experimental results validated the effectiveness of this approach, with energy savings up to 45% and minimal accuracy loss across CNN and transformer benchmarks. The findings highlight the importance of holistic circuit-level strategies in shaping the next generation of AI hardware, paving the way for scalable, low-power, and thermally sustainable accelerators suitable for mobile and IoT devices.

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